ST-BUS Generic Device Specification (Rev. B)

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Contents

1.0 Introduction

As systems become more complex, the trend in system design has been to partition circuitry into well defined functional blocks. Such partitioning localizes circuitry performing a particular function to a specific location in a system, thus promoting modularity. Modularity is an important consideration, particularly for flexibility in system configuration. Modularity is also a good defence against obsolescence. The amount of investment in a system design makes it expensive to throw away, especially when only portions may be outdated. This is avoided by improving the outdated portions and keeping the rest of the system. These design philosophies can only be implemented if the system is designed modularly from the beginning.

It is necessary to have a well defined, effective means of communication and information transfer between modules (the term information is used here because it can apply equally to audio, video, control information or data). The definition of a common interface between functional blocks eases the addition of new circuitry to a design. Such an interface should be simple, to allow modules to have a wide range of complexity. The interface should be capable of being overlayed by higher levels of communication protocol such as High Level Data Link Control (HDLC), for instances where communication needs are more demanding. There is no need to constrain module design where such a protocol is not needed.

Mitel Semiconductor has defined the ST-BUS (Serial Telecom Bus) with the above requirements in mind. It is simple to interface to, and can handle all four types of information mentioned, when the information is digitized. The ST-BUS Generic Device Specification presented in Tables 1 and 2 of this document encompasses the “worst case” timing parameters of the ST-BUS interface for different data rates. New ST-BUS compatible components or circuits must conform to these minimum and maximum timing specifications, or be better, to ensure compatibility with all components and systems that already exist. A system designer may use these overall component timing specifications to aid in the interconnection of ST-BUS devices.

2.0 ST-BUS Form and Signals

The ST-BUS is a high speed, synchronous serial bus for transporting information in a digital format. The use of serial streams minimizes the printed circuit board area needed for information transfer between functional modules. Fewer tracks, backplane connections, and intra-shelf cables are needed compared to systems that use parallel paths. These considerations become critical in systems that have a high information flow density, with many simultaneous communications occurring between functional modules. At the integrated circuit level, the benefits of using a serial interface on an IC are reduced pin count, improved reliability and decreased power dissipation.

The signals required to interface to the ST-BUS are:

i) A framing signal for frame alignment
ii) A clock signal for bit timing
iii) Serial information streams

Depending on the application, the aggregate rate of the ST-BUS information stream can be 2.048, 4.096 or 8.192 Mbit/s. This stream is divided into frames, each frame having a period of 125 µs, for a frame rate of 8000 frames/s. The start of each ST-BUS frame is indicated by the framing signal (frame pulse). Each frame is divided into an integer number of bit periods, with bit timing provided by the clock signal (see Figure 1). This information stream could be considered a single high speed communication channel between two points, however, the full digital bandwidth is not needed for many applications. It is therefore useful to divide this high speed channel into multiple, lower bandwidth channels. This makes it possible to share the capacity of one serial ST-BUS stream among several channels, referenced to the

frame pulse, to improve system efficiency and economy. This technique is called Time Division Multiplexing (TDM).

As an example of a lower bandwidth requirement, transferring voice down a digital channel in a telecommunications application requires a digital bandwidth of 64 kbit/s. This value is obtained from the following facts about digitizing voice:

a/ The normal voice band has an upper frequency bound of 3.5 kHz to 4 kHz, through the telephone network.

b/ Voice may be translated to digital format by taking a sample of the analog voice signal and producing an eight bit code from the sample. One type of encoding is called Pulse Code Modulation (PCM). An eight bit PCM sample contains polarity and amplitude information.

c/ All the information in the original analog signal can be replicated from the digital information if enough samples are taken. To retain all of the information, sampling must be performed at twice the highest frequency contained in the signal being digitized. In this case sampling must be performed at 8 kHz. 8000 samples of eight bits each, per second, is 64 kbit/s; the digital bandwidth of normal voice transmitted through the public telephone network.

Note that the sampling rate for voice is equivalent to the frame rate of the ST-BUS. For example, if an ST-BUS frame at 2.048 Mb/s was divided into eight bit bytes, one ST-BUS frame could contain 32 of these portions, equivalent to 32 PCM encoded voice samples. This translates into 32 channels with a 64 kbit/s digital bandwidth, enough for 32 simultaneous digitized voice channels. See Figure 1 for a typical representation of an ST-BUS frame at 2.048, 4.096 and 8.192 Mbit/s, respectively, and how it may be divided into sub-channels (in this instance 64 kbit/s channels).

For a number of different nodes to source information onto a single ST-BUS stream, three-state buffers must be used. All outputs but one must be in the high impedance state, so that no more than one device drives the bus at a time. The upper bound on the number of sources is determined by definition of the number of channels, the output drive of the source node with the least current driving capability, and the capacitance of the track and/or wire on which the stream is carried.

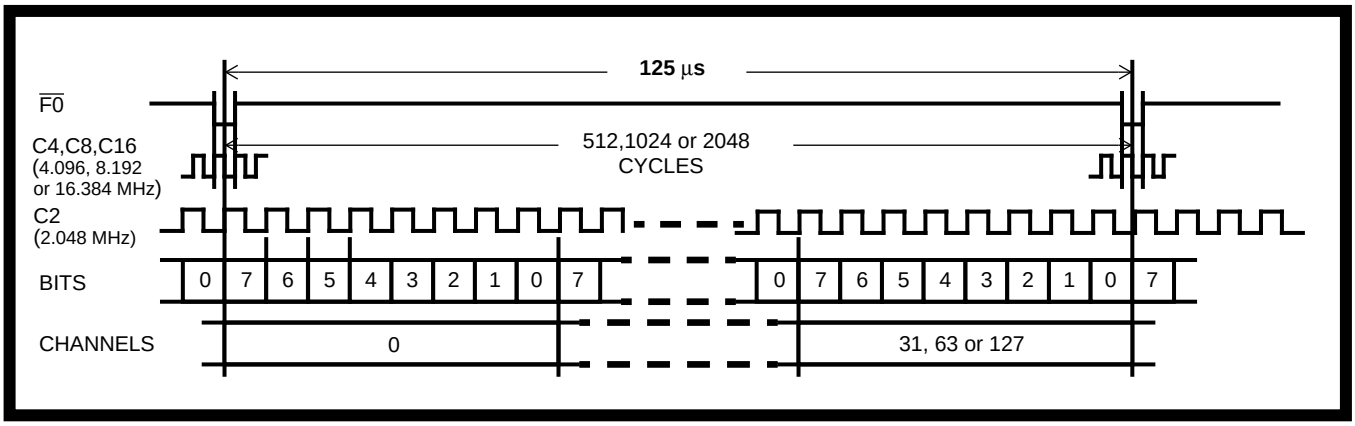


Figure 1 - $\overline{F0}$ and Clock Alignment for ST-BUS at 2.048 Mb/s, 4.096 and 8.192 Mb/s

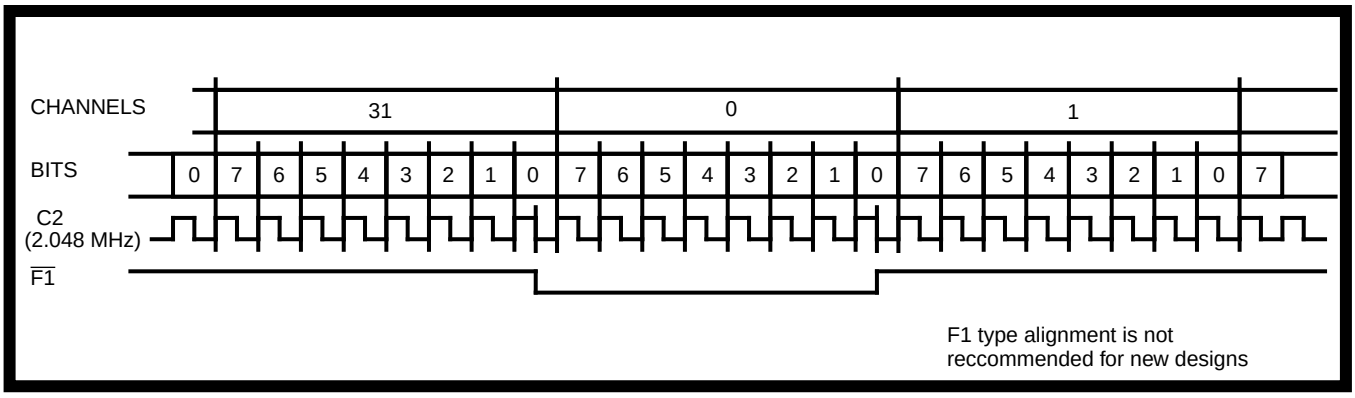


Figure 2 - Example of $\overline{F1}$ Alignment for ST-BUS at 2.048 Mb/s

The number of receivers on one ST-BUS stream is also limited by the source node with the least output drive capability, and by the capacitance of the wire and/or track carrying the stream. Access to a particular channel or channels is achieved by referencing the frame pulse and using the clock signal to position the access.

3.0 Clocking Signals

The ST-BUS defines four standard clock frequencies. Each one can be used for supplying ST-BUS components' internal timing needs, but only one is required at any one time by a particular component (some components can be designed to automatically select the clock speed). The currently defined clock frequencies are 16.384, 8.192, 4.096 and 2.048 MHz.

Clock frequencies are always twice the data rate except for 2.048 MHz. For devices operating at 2.048 Mbit/s data rates, either 2.048 or 4.096 MHz clocks can be used as depicted in Figures 1 and 3.

4.0 Alignment Signals

Alignment Signals for ST-BUS at 2.048 Mbit/s

There are two main types of alignment signals (also called Frame Pulses). One type is a pulse that always occurs at the start of a frame (Type 0) as per Figure 1. ST-BUS components that use this signal use it as a reference and then use the clock input to determine when to receive or transmit information on the serial stream.

The other type of Frame Pulse (Type 1) is similar to a chip enable (Figures 2 and 4). This pulse must span the entire ST-BUS channel time in which an ST-BUS component is to receive or transmit serial information. F1 type frame pulse is not recommended for new designs.

For higher rate ST-BUS frames, Type 0 frame alignment signals are only applicable.

5.0 Information Streams

The information stream is the serial stream on which information is carried between ST-BUS components. An information stream can be output entirely from one device, or built up from the individual channel outputs of multiple devices (for example: a number of MT8960 Voice Codecs, or multiple MT8985 Digital Switches). Most ST-BUS components transmit status information and receive control information, as well as information for processing, on ST-BUS information streams.

In certain applications, the ST-BUS streams are required to have bidirectional operation on a per time-slot basis. This function is a device specific feature and the overall AC Electrical Characteristics have to comply with the limits given in Tables 1 and 2.

6.0 Worst Case Timing Parameters

Tables 1 and 2 contain the worst case timing parameters for 2.048, 4.096 and 8.192 Mbit/s, respectively. Devices may be better than this specification, but they should be no worse. The definition of what is better or worse is dependent on the perspective taken, so several typical examples shall be described to clarify this.

For applications at 2.048 Mbit/s where 4.096 MHz clock is employed the typical C4 clock period is 244.1 ns. The smallest range about this typical value that can be tolerated by any of the existing ST-BUS devices is from a minimum of 243.9 ns to a maximum of 244.4 ns. No ST-BUS device can have a narrower range than this, however, a wider range is acceptable (eg., minimum 240 ns to maximum 250 ns). A system designer can be sure that if a clock is provided with a tolerance that is within the worst case tolerances in Table 1 for C4, it will be good enough for all ST-BUS devices operating at 2.048 Mbit/s.

The perspective is similar for other parameters with both a minimum and a maximum specified, except for the STo Delay. For STo Delay, there is an acceptable window that no device may be outside of. There are three values of STo Delay, distinguished by load capacitance for each ST-BUS data rate employed. This reflects the varying drive requirements of ST-BUS devices. Almost all ST-BUS devices available from Mitel Semiconductor at present have Level 2 STo outputs (see Tables 1 and 2).

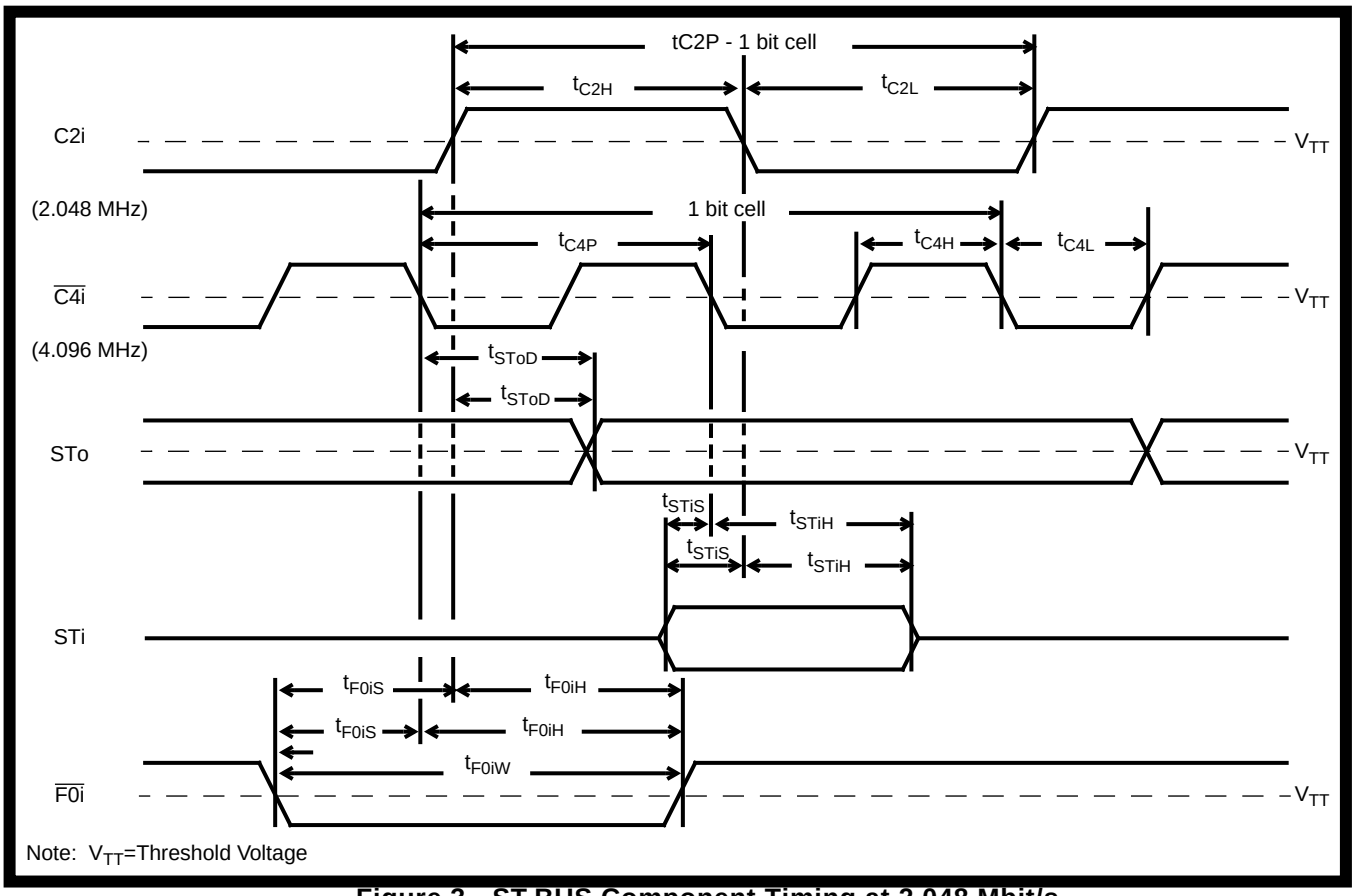


Figure 3 - ST-BUS Component Timing at 2.048 Mbit/s

	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Clock C4 Period*	t_{C4P}	243.9	244.1	244.4	ns	
2	Clock C4 High Width	t_{C4H}	110	122	134	ns	
3	Clock C4 Low Width	t_{C4L}	110	122	134	ns	
4	Clock C2 Period*	t_{C2P}	487.8	488.3	488.8	ns	
5	Clock C2 High Width	t_{C2H}	220	244	268	ns	
6	Clock C2 Low Width	t_{C2L}	220	244	268	ns	
7	$\overline{F0i}$ Setup Time	t_{F0iS}	50 ①		150	ns	
8	$\overline{F0i}$ Hold Time	t_{F0iH}	50 ①		150	ns	
9	$\overline{F1i}$ Setup Time	t_{F1iS}	50 ①		150	ns	
10	$\overline{F1i}$ Hold Time	t_{F1iH}	50 ①		150	ns	
11	$\overline{F0i}$ Width	t_{F0iW}	200		300	ns	
12	$\overline{F1i}$ Width	t_{F1iW}	3.903		3.910	µs	
13	STo Delay Level 1 Output	t_{SToD}	20	90	125	ns	C_L= 50 pF
14	STo Delay Level 2 Output	t_{SToD}	20	90	125	ns	C_L= 150 pF
15	STo Delay Level 3 Output	tstoD	20	90	125	ns	C_L= 200 pF
16	STi Set Up Time	t_{STiS}	30			ns	
17	STi Hold Time	t_{STiH}	224			ns	

Table 1. Worst Case Component Timing† Specification for 2.048 Mb/s Streams

† Timing is over recommended temperature range (-40 °C to 85 °C) and recommended voltage range (5 V±5%)
* These tolerances are required by voice codecs to meet CCITT G.712 Method 2. Other devices have less stringent requirements.
① Recommended values for new designs is set to 20ns minimum.

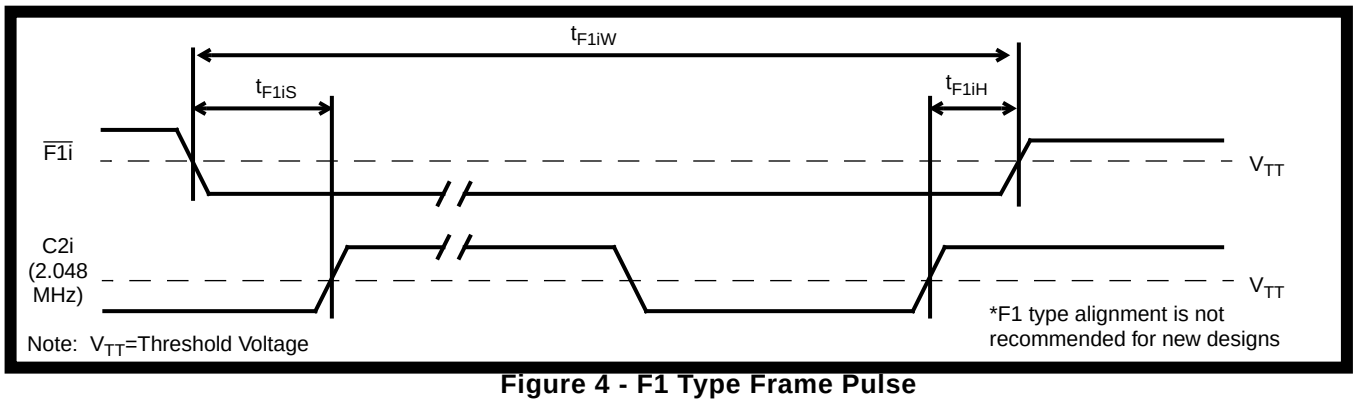


Figure 4 - F1 Type Frame Pulse

For the next two parameters in the table (STi Setup Time and STi Hold Time), it is acceptable for a device to have smaller minimums, but not to have larger minimums. In applications at 2.048 Mb/s, the ST-BUS device inputs can be either sampled at the halfway point in a bit cell or at the three quarter point in a bit cell. For applications at 4.096 and 8.192 Mb/s the ST-BUS inputs are sampled at three quarters of the bits cell.

The STi Setup and Hold times for 2.048 Mb/s shown in Table 1 are with respect to the halfway point in the bit cell, and are defined to accommodate both sampling points. Devices that are sampled at the half way point will generally have better STi Hold Times (smaller than 224 ns) and devices sampled at the three quarter point will have better STi Setup Times (less than 30 ns; usually negative).

7.0 Nomenclature

A nomenclature has been created to quickly identify ST-BUS signals

7.1 Clock Signals

A bar above a clock name means that the clock has a falling edge at the frame boundary. Examples of clock signals are C4i, C2i, E8Ko etc. The meaning of each letter or digit in the clock name is as follows:

1) Clock Type

C - ST-BUS system clock.

E - extracted or derived clock associated in some way with a received digital trunk or line.

2) Frequency

Approximate frequency in megahertz (kilohertz if K added).

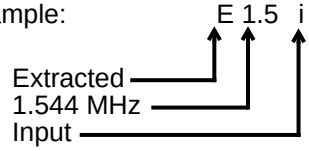
3) I/O Type

i - Input.

o - Output.

b - Bidirectional.

Example: E 1.5 i



7.2 Framing Signals

A bar above a signal name means that the signal is active low. Some examples of Framing Pulse names are F0i, F1o. The meaning of each letter or digit in the name is as follows:

1) First Letter

F - denotes a framing signal.

2) Framing Type Number

0,1,2,... - There is a variety of these signals, each with distinctive properties, conforming to no simple pattern.

3) I/O Type

i - Input.

o - Output.

b - Bidirectional.

4) Optional Suffix

d - Delayed

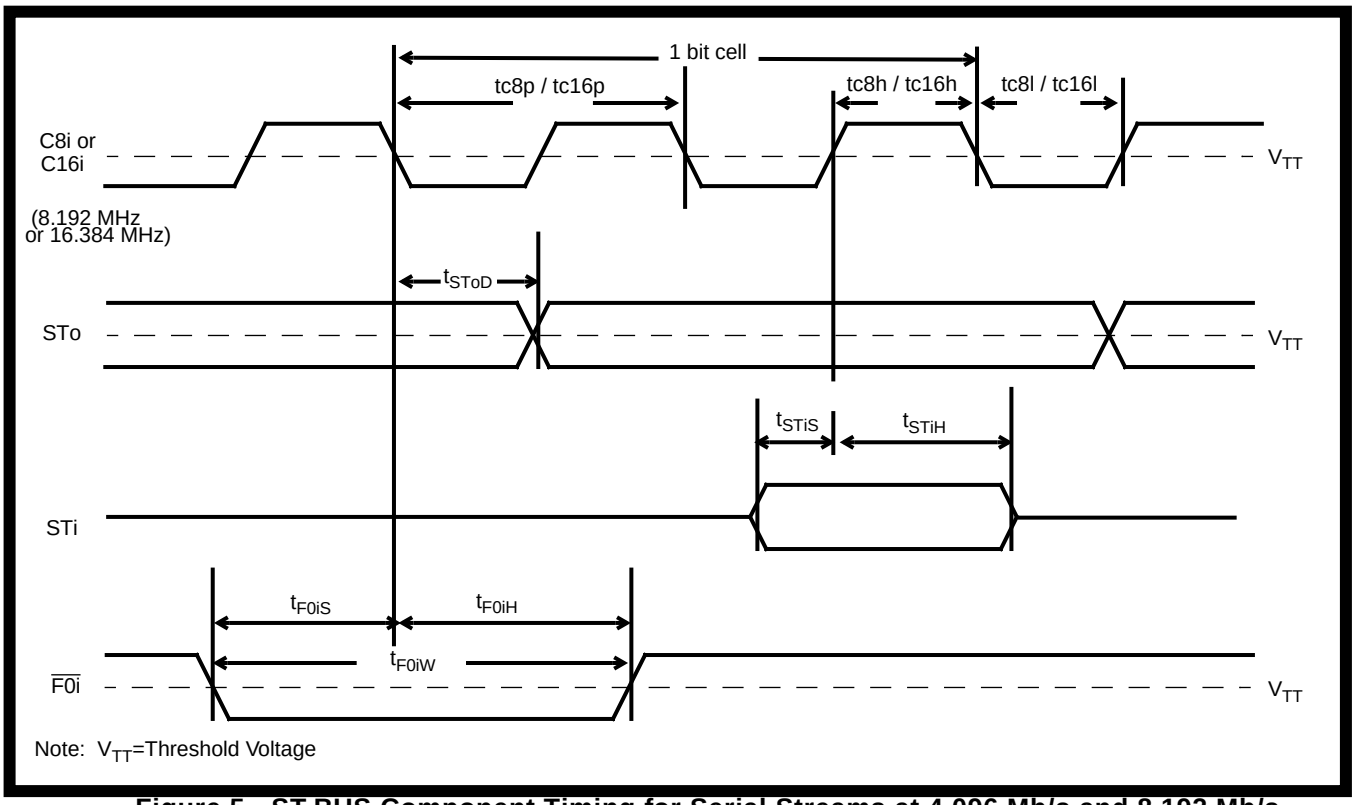


Figure 5 - ST-BUS Component Timing for Serial Streams at 4.096 Mb/s and 8.192 Mb/s

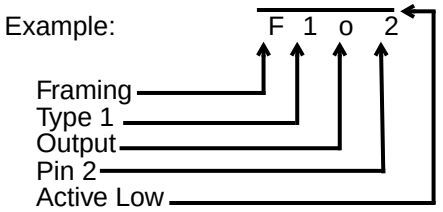
	Characteristic	Sym	Min	Typ	Max	Units	Test Conditions
1	Clock Period**	tc8p tc16p	110 54	122.1 60	134 66	ns	for 4.096 Mb/s for 8.192 Mb/s
2	Clock High Width	tc8h tc16h	55 27	61 30	67 33	ns	for 4.096 Mb/s for 8.192 Mb/s
3	Clock Low Width	tc8l tc16l	55 27	61 30	67 33	ns	for 4.096 Mb/s for 8.192 Mb/s
4	$\overline{F0i}$ Setup Time	t_{F0iS}	20			ns	
5	$\overline{F0i}$ Hold Time	t_{F0iH}	20			ns	
6	$\overline{F0i}$ Width	t_{F0iW}	50			ns	
7	STo Delay Level 1 Output for 4.096 Mb/s for 8.192 Mb/s	t_{SToD}			 80 45	ns	C_L= 50 pF
8	STo Delay Level 2 Output for 4.096 Mb/s for 8.192 Mb/s	t_{SToD}			 80 45	ns	C_L= 150 pF
9	STo Delay Level 3 Output for 4.096 Mb/s for 8.192 Mb/s	tstod			 80 45		C_L = 200 pF
10	STi Set Up Time for 4.096 Mb/s for 8.192 Mb/s	t_{STiS}	 20 5			ns	
11	STi Hold Time for 4.096 Mb/s for 8.192 Mb/s	t_{STiH}	 30 20		 180 90	ns	

Table 2. Worst Case Component Timing† Specification for 4.096 Mb/s and 8.192 Mb/s Streams

† Timing is over recommended temperature range (-40 °C to 85 °C) and recommended voltage range (5 V±5%)
** For systems using Voice Codecs meeting CCITT G.712 Method 2, t_{C4P} should comply with the values described in Table 1.

5) Pin Number

0,1,2,... - distinguishes between different device ports for similar signals.



7.3 ST-BUS Streams

Some examples of ST-BUS stream names are STi0, STo1, CSTo, etc. The meaning of each letter or digit in the name is as follows:

1) Optional Prefix

C - control.
D - data or PCM encoded voice.

NB: No prefix if stream function not pre-assigned.

2) Type Letters

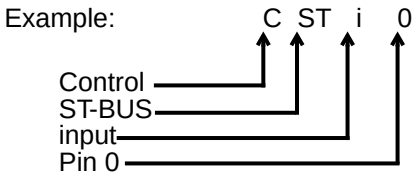
ST - denotes ST-BUS information stream.

3) I/O Type

i - Input.
o - Output.
b - Bidirectional.

4) Pin Number

0,1,2 - distinguishes between different logical ports for similar signals.



Notes: